FIG.1

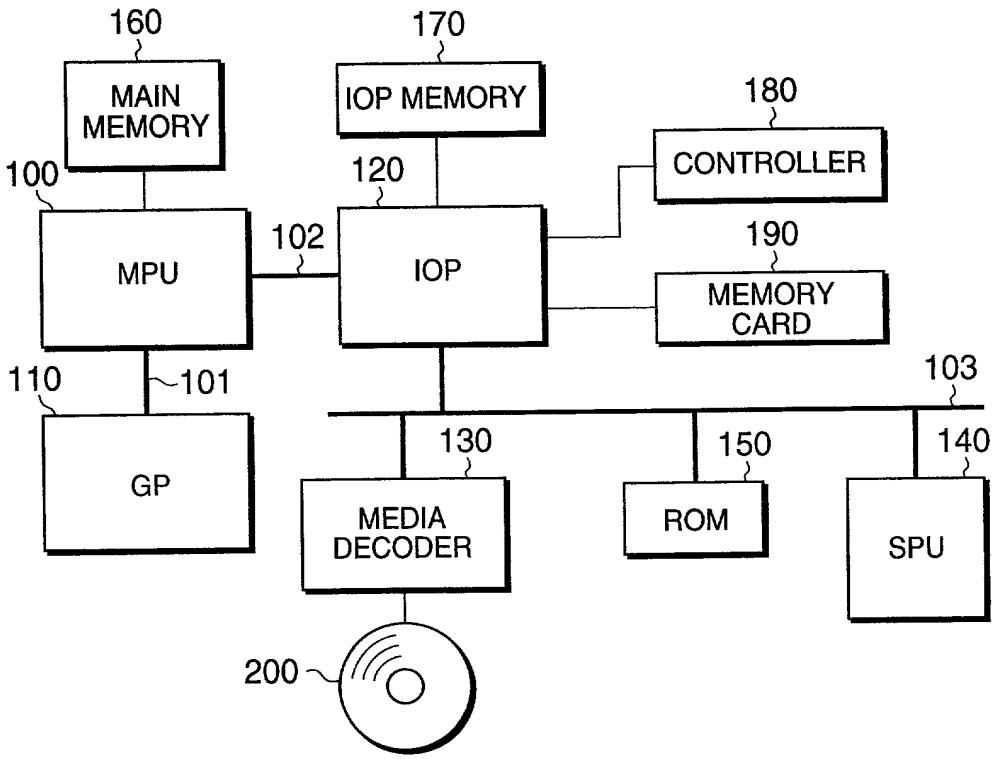
160
MAIN MEMORY
170
IOP MEMORY
180
CONTROLLER
100
120
MPU
102
IOP
190
MEMORY CARD
110
101
103
GP
130
150
140
MEDIA DECODER
ROM
SPU
200

FIG.2

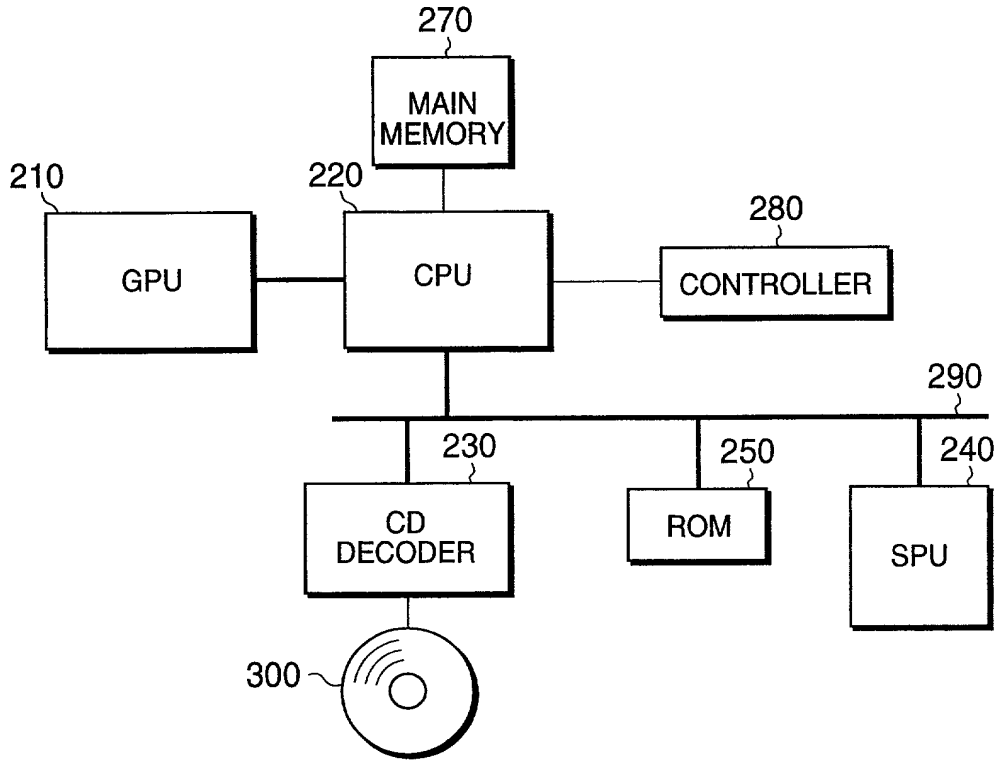
270
MAIN MEMORY
210
220
280
GPU
CPU
CONTROLLER
290
230
250
240
CD DECODER
ROM
SPU
300

FIG.3

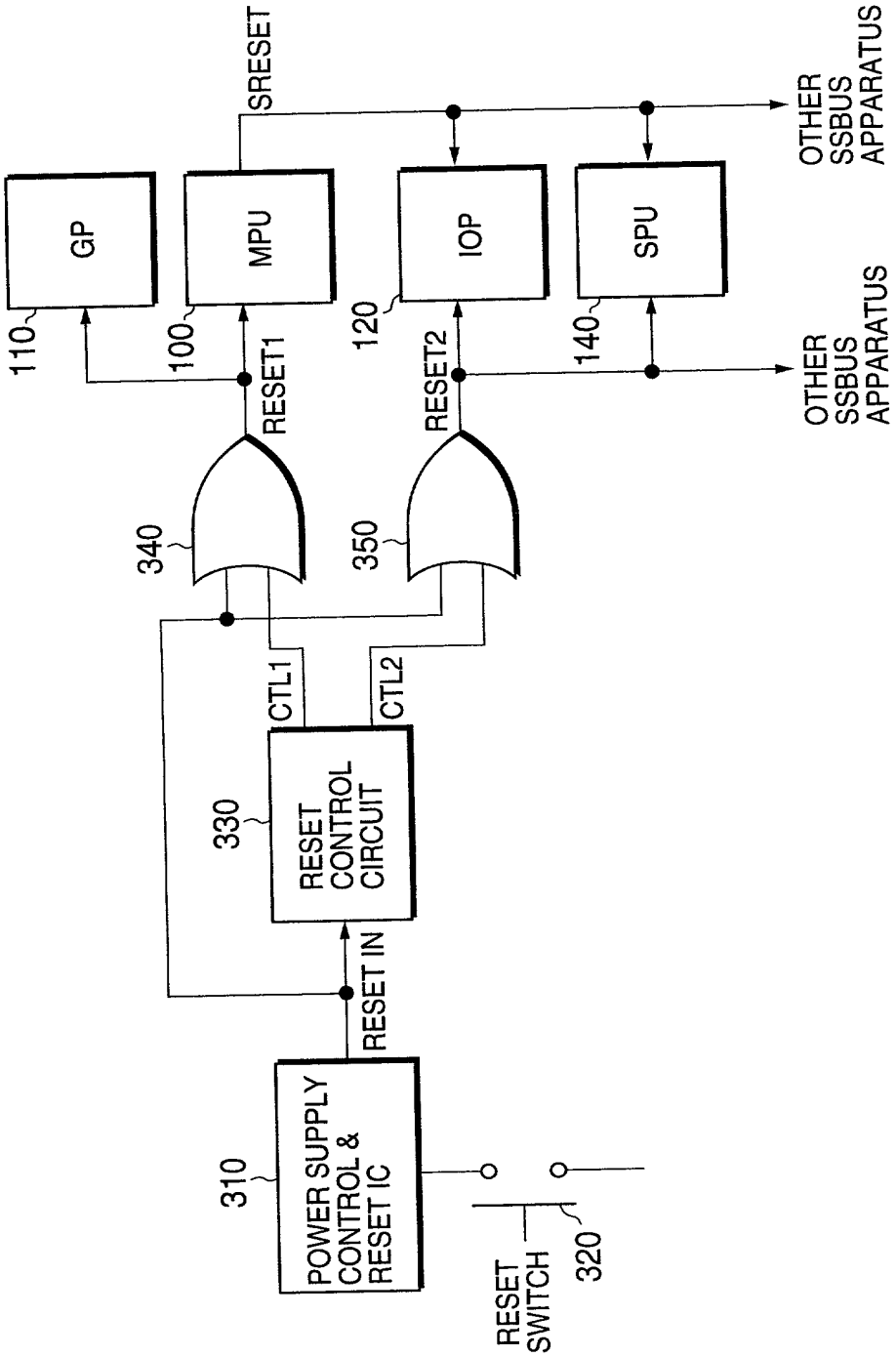
POWER SUPPLY CONTROL & RESET IC
310
RESET SWITCH
320
RESET IN
RESET CONTROL CIRCUIT
330
CTL1
CTL2
340
350
RESET1
RESET2
SRESET
GP
110
MPU
100
IOP
120
SPU
140
OTHER SSBUS APPARATUS
OTHER SSBUS APPARATUS

FIG.4

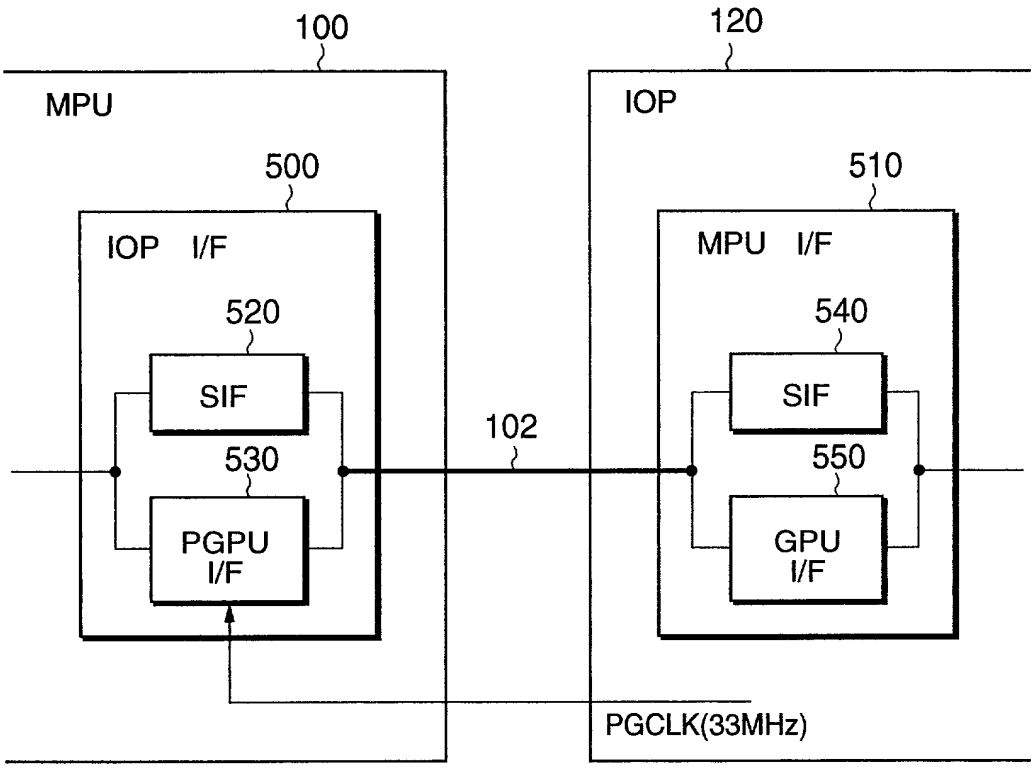
100
MPU
500
IOP I/F
520
SIF
530
PGPU I/F
102
120
IOP
510
MPU I/F
540
SIF
550
GPU I/F
PGCLK(33MHz)

FIG.5

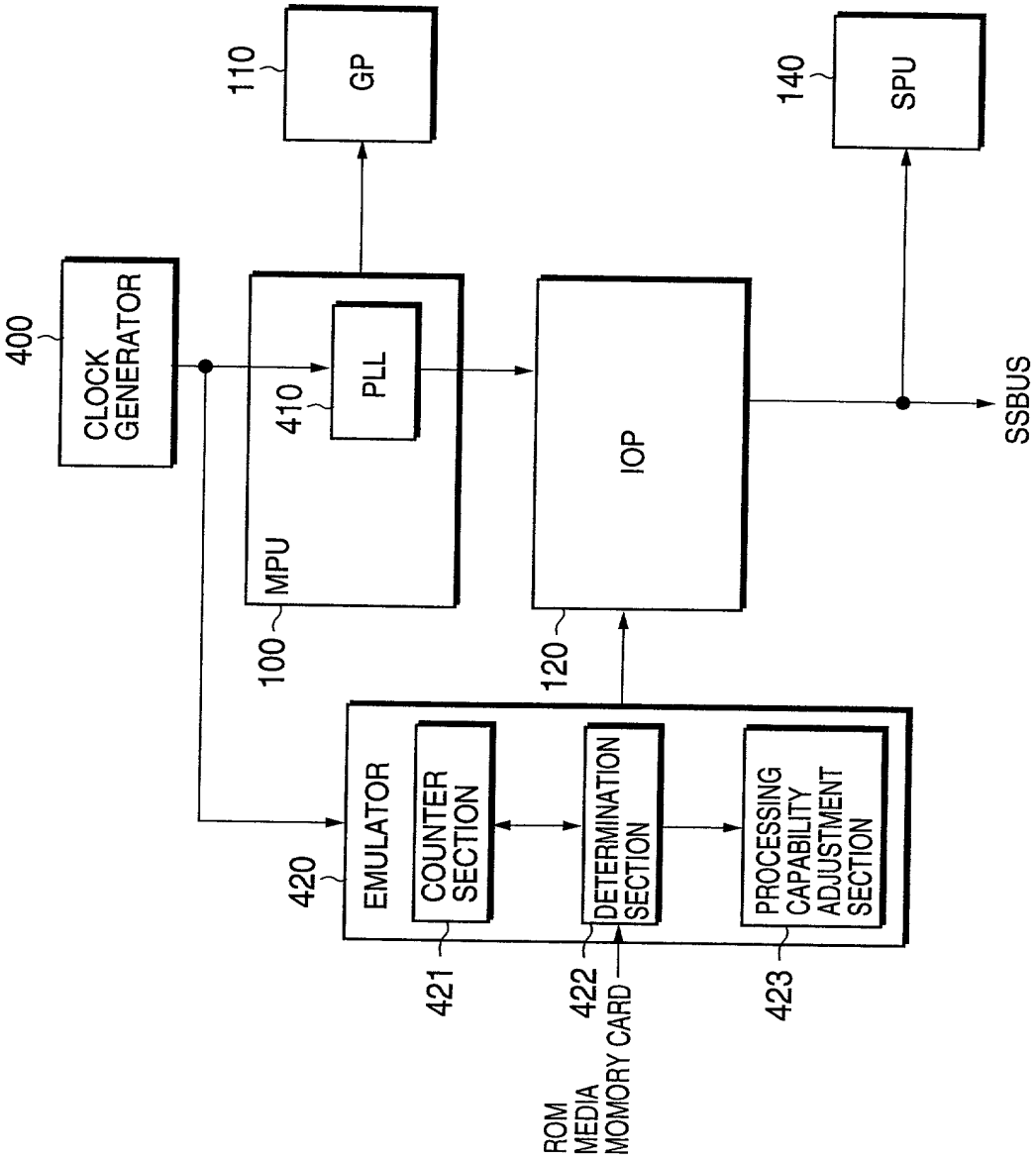
400
CLOCK GENERATOR
110
GP
140
SPU
410
PLL
MPU
100
IOP
120
SSBUS
420
EMULATOR
COUNTER SECTION
DETERMINATION SECTION
PROCESSING CAPABILITY ADJUSTMENT SECTION
421
422
423
ROM MEDIA MOMORY CARD

FIG.6A

ADJUSTMENT TARGET TITLE	POLYGON DRAWING SPEED	SPRITE DRAWING SPEED	-----
AAA	0	2	-----
BBB	0	1	-----
⋮	⋮	⋮	-----

FIG.6B

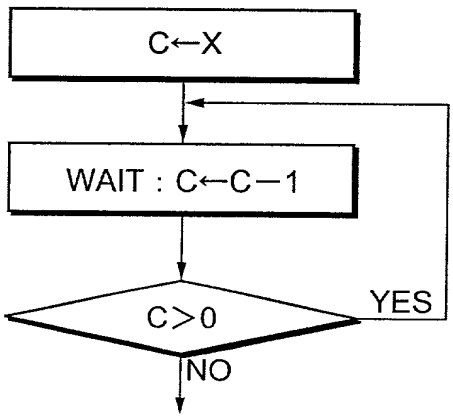

FIG.7

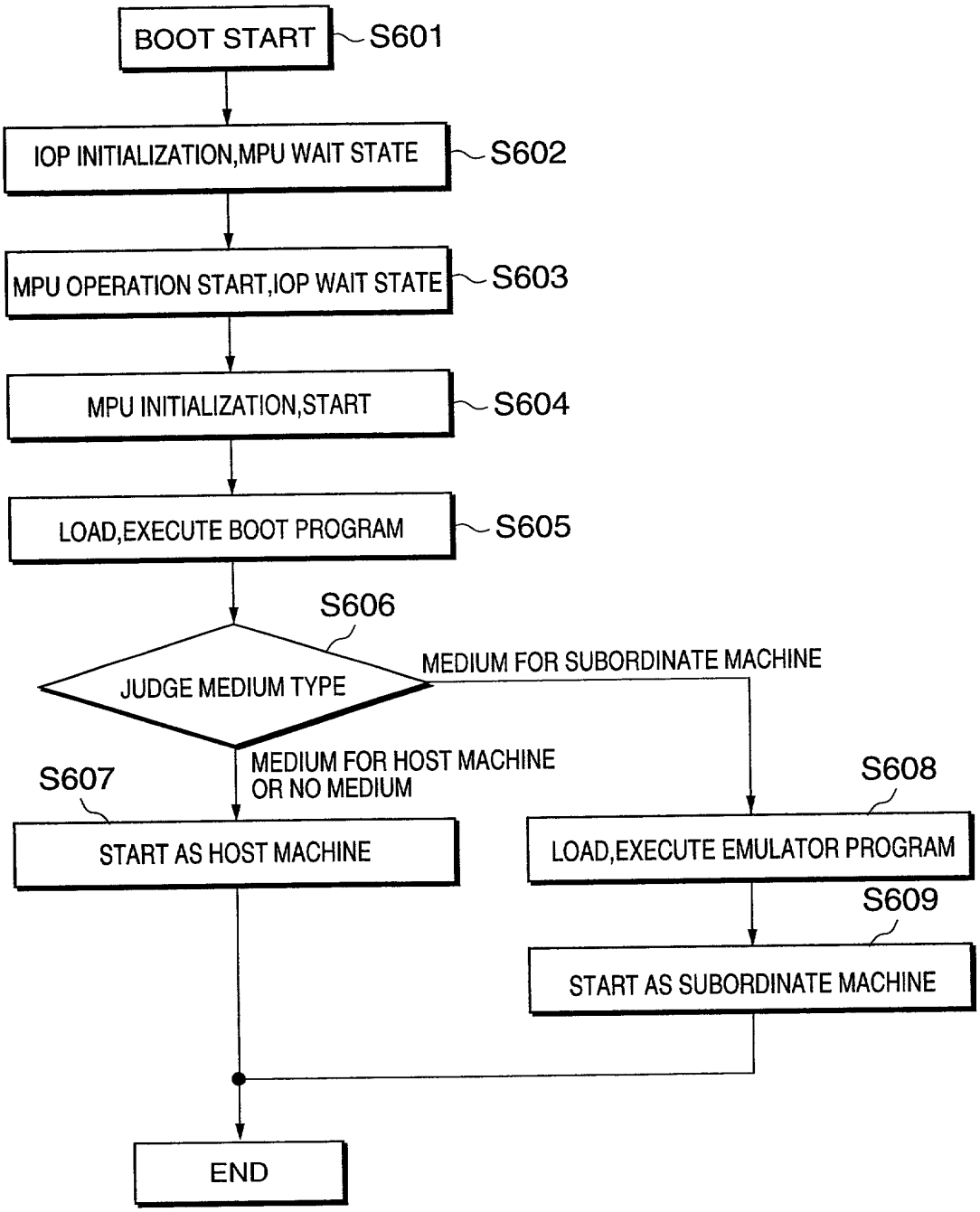
BOOT START
S601
IOP INITIALIZATION,MPU WAIT STATE
S602
MPU OPERATION START,IOP WAIT STATE
S603
MPU INITIALIZATION,START
S604
LOAD,EXECUTE BOOT PROGRAM
S605
S606
JUDGE MEDIUM TYPE
MEDIUM FOR SUBORDINATE MACHINE
MEDIUM FOR HOST MACHINE
OR NO MEDIUM
S607
START AS HOST MACHINE
S608
LOAD,EXECUTE EMULATOR PROGRAM
S609
START AS SUBORDINATE MACHINE
END

FIG.8

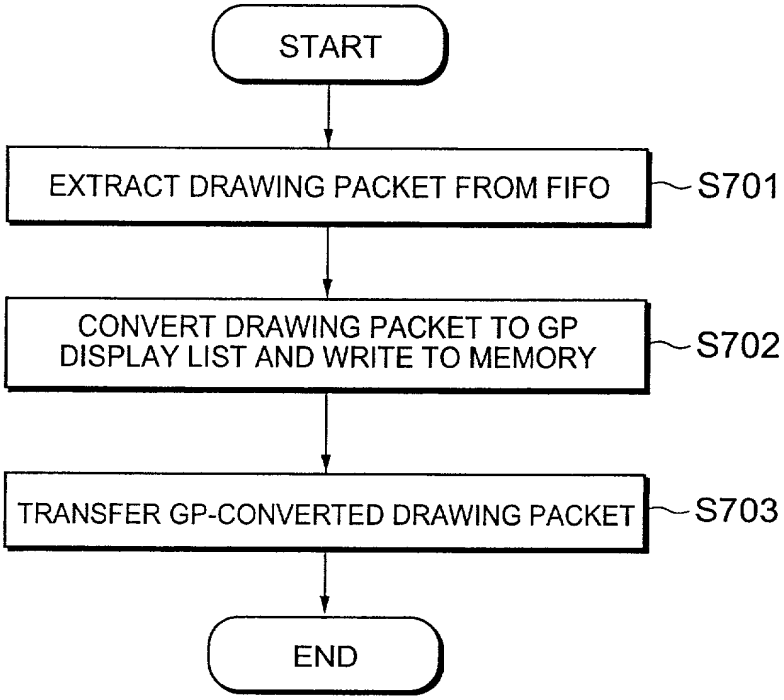

FIG.9A

Code	B	G	R
Y0		X0	
Y1		X1	
Y2		X2	

FIG.9B

Code				
			B	G	R
	Z2	Y0		X0	
	Z2	Y1		X1	
	Z2	Y2		X2	